IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) An apparatus comprising:

a first processor having two or more processor elements and two or more input/output (I/O) ports coupled together by a first port ring that is within the first processor; and

a second processor having two or more processor elements and two or more I/O ports coupled together by a second port ring that is within the second processor, wherein the second processor is coupled to the first processor through at least one I/O port of a third port ring within a third processor, wherein the two or more I/O ports in the first processor, the second processor and the third processor are configured to establish a logical connection between the first processor and the second processor, the logical connection to originate at first processor and to traverse through the third processor and to complete at the second processor, wherein the logical connection is established based on other active logical connections that include at least one of the first processor, the second processor and third processor.

2. (Previously Presented) The apparatus of claim 1, wherein the two or more I/O ports of the first processor is not directly connected to the two or more I/O ports of the second processor.

3. (Original) The apparatus of claim 1, wherein the first processor, the second processor and the third processor are part of a number of processors in a point-to-point configuration.

4. (Original) The apparatus of claim 1, wherein the first processor is configured to transmit output from an image process operation to the second processor through the at least one I/O port of the port ring of the third processor based on a logical connection.

5. (Previously Presented) The apparatus of claim 4, wherein the two or more I/O ports of the first processor, the two or more I/O ports of the second processor and the at least one I/O port of the third processor comprise a First-In-First-Out memory.

6. (Previously Presented) The apparatus of claim 5, wherein the two or more I/O ports of the first processor, the two or more I/O ports of the second processor and the at least one port of the third processor comprise a receiver port and a transmitter port, wherein the first processor is configured to transmit the output based on a handshake protocol among the receiver ports and the transmitter ports of the first processor, the second processor and the third processor.

7. (Previously Presented) An apparatus comprising:

a number of image signal processors coupled together in a point-to-point configuration, wherein one image signal processor of the number of image signal processors includes at least one processor element and a port ring, wherein the port ring includes a number of ports, a port of the number of ports coupled to the other ports of the port ring and to a port of a port ring of a different image signal processor, wherein the number of ports within the port rings of the number of image signal processors are configured to establish logical connections between the number of image signal processors, wherein the logical connections are to originate at a source image signal processor of the number of image signal processors and to traverse a number of intermediate image signal processors of the number of image signal processors and to complete at a destination image signal processor of the number of image signal processors, wherein the source image signal processor is to transmit an initialize signal, prior to transmission of data along the logical connection, through the number of intermediate image signal processors to the destination image signal processor in the order that data is transmitted in the logical connection.

8. (Original) The apparatus of claim 7, wherein the at least one processor element in a first of the number of image signal processors is configured to perform one of a number of image process-based operations.

9. (Canceled).

10. (Previously Presented) The apparatus of claim 9, wherein the at least one processor element is configured to output a result of the one of the number of image process-based operations to a different processor element in a different image signal processor through one of the logical connections.

11. (Canceled).

12. (Original) The apparatus of claim 9, wherein the number of ports include a storage memory for storage of data between communicated among the number of image processors through the configured logical connections.

13. (Previously Presented) A system comprising:

a Complementary Metal Oxide Semiconductor (CMOS) sensor to capture image data;

an image processor comprising a number of expansion interfaces and a number of image signal processors, wherein at least one expansion interface of the number of expansion interfaces is configured to receive the image data to be captured by the CMOS sensor, wherein at least one image signal processor of the number of image signal processors comprises a processor element and a port ring having a number of input/output ports to couple the at least one image signal processor to other image signal processors in the image processor in a point-to-point configuration; and

a host processor to configure a number of logical connections among the number of image signal processors, wherein at least one logical connection is to originate at a source image signal processor of the number of image signal processors and to finish at a destination image signal processor of the number of image signal processors, wherein the at least one logical connection includes traversal through a number of ports of the port rings of at least one intermediate image signal processor of the number of image signal processors between the source image signal processor and the destination image signal processor.

14. (Original) The system of claim 13, wherein the at least one image signal processor comprises a hardware accelerator to execute image process operations.

15. (Original) The system of claim 13, wherein the image processor comprises a global bus coupled to the number of expansion interfaces and the number of image signal processors, independent of the point-to-point configuration among the number of image signal processors.

16. (Canceled)

17. (Original) The system of claim 13, wherein traversal through the number of ports of the port rings of the at least one intermediate image signal processor is independent of image process operations by processor elements within the at least one intermediate image signal processor.

18. (Previously Presented) A method comprising:

registering a logical connection with a number of ports of port rings of a number of image signal processors in a logical connection based on transmission of an initialization signal through the logical connection;

executing an image process operation; and

forwarding an output of the image process operation through the logical connection that includes a data path through the number of ports of port rings of the number of image signal processors, independent of image process operations in the number of image signal processors.

19. (Original) The method of claim 18, wherein forwarding the output of the image process operation through the logical connection from one of the number of image signal processors to a different one of the number of image signal processors comprises,

transmitting a request signal from a transmitter port of the one of the number of image signal processors to a receiver port of the different one of the number of image signal processors; and

receiving, in response to the request signal, a grant signal from the receiver port to the transmitter port.

20. (Canceled)

21. (Original) The method of claim 18, wherein forwarding the output of the image process operation through the logical connection that includes the data path through the number of ports of the port rings of the number of image signal processors comprises forwarding the output of the image process operation through the logical connection that includes the data path through the number of ports of the port rings of the number of image signal processors, wherein the number of image signal processors are connected together through the number of ports in a point-to-point configuration.

22. (Original) A method comprising:

receiving configuration data for a logical connection established for transmission of image data from a source image signal processor to a destination image signal processor through a number of intermediate image signal processors;

registering the logical connection with ports of the source image signal processor, the destination image signal processor and the number of intermediate image signal processors; and

routing the image data through the ports of the logical connection, subsequent to registering the logical connection and independent of image process operations by processing elements within the number of intermediate image signal processors.

23. (Original) The method of claim 22, wherein registering the logical connection with the ports of the source image signal processor, the destination image signal processor and the number of intermediate image signal processors comprises transmitting an initialize signal that is transmitted along a path of the logical connection that the image data is routed.

24. (Original) The method of claim 22, wherein registering the logical connection with the ports of the source image signal processor, the destination image signal processor and the number of intermediate image signal processors comprises registering point-to-point connections between the ports of the logical connection.

25 -30. (Canceled).